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Project 1 report

The logic for the seven-segment display was derived from the truth table given. Using the minterms from the truth table, I was able to use Karnaugh maps to find the equation for each segment. The equations were all sums of products, therefore it’s a group of “and” gates that are then all put as inputs into an “or” gate. For the Verilog code, I divided up the equation for each segment into the products and used “and” gates to get the output. This output was stored in wires and all the wires that held the outputs of the “and” gates for that segment. These outputs were then put as inputs for an “or” gate which was stored in the final output for that segment. This process was repeated for the remaining segments in the seven-segment display module. In the test bench module, I create four logic switches that represent the four inputs to the whole system and seven wires that represent each segment. These switches and wires are then used to call the seven-segment display module using them as the inputs to the function. The remaining code of the test bench is a loop that repeats the function call until it has run a total of sixteen times to account for all the combinations of the four inputs.





